ABSTRACT

A programmable system and a self-locking memory circuit for a tri state data bus having multiple bit lines. The circuit includes a non-inverting amplifier chip for connection to one of the bit lines and a resistor having a predetermined electrical resistance connected across the amplifier chip. The chip and resistor provide a predetermined impedance to the flow of electrical current in the self-locking circuit. The circuit changes its state when the current of the latest information on a bit line builds or lowers above or below threshold levels of the self-locking circuit. The tri state data bus may be connected between a digital signal processor (DSP), a complex programmable logic device (CPLD) and a central processing unit (CPU) operating at different rates or speeds.